a. a synchronous portion, disposed to receive and respond to a clocked signal;

b. an asynchronous portion, coupled with a line for the memory cell; and

c. a feedback-resetting portion, coupled with the synchronous portion and the asynchronous portion and interposed there between, the feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion responsive to an asynchronous reset signal.

2. (Amended) The decoder of Claim 1, wherein the feedback-resetting portion substantially isolates the synchronous portion from the asynchronous portion responsive to a monitor signal.

6. (Amended) A decoder in a memory module having a plurality of memory cell groups, comprising:

a. a signal input;

b. a first memory output coupled with a first memory cell group;

c. a second memory output coupled with a second memory cell group; and

d. a selector coupled between the signal input, the first memory output, and the second memory output, wherein the decoder decodes the first memory cell group and being disposed to select and decode the second memory cell group responsive to a group-select signal.

7. (Amended) The decoder of Claim 6, wherein the selector comprises a multiplexer, the multiplexer selecting to decode from one of the first memory

cell group and the second memory cell group, the multiplexer being responsive to the group-select signal.

8. (Amended) The decoder of Claim 6, wherein the decoder is a row decoder disposed in a memory module having a plurality of adjacent memory rows, and wherein a first memory row and a second memory row are adjacent memory rows in the memory module, and the group-select signal is an alternative-row-select signal.

9. (Amended) The decoder of Claim 6, wherein the decoder is a column decoder disposed in a memory module having a plurality of adjacent memory columns, and wherein a first memory column and a second memory column are adjacent memory columns in the memory module, and the group-select signal is an alternative-column-select signal.

12. (Amended) A decoder in a memory module having a plurality of memory cell groups, comprising:

a. a synchronous portion, disposed to receive and respond to a clocked signal;

b. an asynchronous portion, coupled with a selected memory cell group;

c. a feedback-resetting portion, coupled with the synchronous portion and the asynchronous portion and interposed there between, the feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion responsive to an asynchronous reset signal;

d. a signal input;

e. a first memory output coupled with a first memory cell group;

f. a second memory output coupled with a second memory cell group; and

g. a selector coupled between the signal input, the first memory output, and the second memory output, wherein the decoder decodes the first memory cell group, and being disposed to select and decode the second memory cell group responsive to a group-select signal.

13. (Amended) The decoder of Claim 12, wherein the selector comprises a multiplexer, the multiplexer selecting to decode from one of the first memory cell group and the second memory cell group, the multiplexer being responsive to the group-select signal.

14. (Amended) The decoder of Claim 12, wherein the decoder is a row decoder disposed in a memory module having a plurality of adjacent memory rows, and wherein a first memory row and a second memory row are adjacent memory rows in the memory module, and the group-select signal is an alternative-row-select signal.

REMARKS

Responding to paragraph 1 of the Office Action, Fig. 1 has been amended to include reference number 125; Fig. 2 has been amended to include reference number 205; Fig. 5 has been amended to include the reference number 512b; Fig. 7 has been amended to include reference terms L0, L1, L2 and M46; the text on page 30, lines 31 and 34 has been corrected to substitute 748 in place of M48 and to substitute 749 in place of M49; Fig. 8 has been amended to include voltage reference Vdd; Fig. 10 has been amended to include reference numbers 1010-1012; page 34 line 18 of the text has

been corrected to substitute 1004 in place of 1013; pages 35-36 have been amended to delete references to M162, M190, M187, M3, M4, M5, M14, M38, M39, M29, M40 and C0; Fig. 14 has been amended to include reference number 1410; page 39 has been amended to substitute "selector device" in place of "redundancy circuit;" Fig. 18 has been amended to include reference numbers 1825 and 1810; Fig. 19 has been amended to include reference number 1900; and pages 49-50 have been amended to delete reference to reset signal 2170 and to delete the term CVS. In summary, the drawings are believed to be in compliance with 37 CFR 1.84(p)(5). Copies of the referenced drawing Figs. with proposed amendments have been provided with this Amendment A.

Responding to paragraph 2 of the Office Action, page 10 and 11 have been amended to include reference to BIT, BIT bar and WORD; COLUMN #1, #2, #N-1 and #N have been deleted from Figs. 3-4; Ccell has been deleted from Fig. 9; pages 37-38 have been amended to include reference to COLUMN PAIR #1-4 AND DECODER # 1-4; page 38 has been amended to include a reference to the "NO CONNECTION" legend in Fig. 15A; page 39 has been amended to substitute "selector device" in place of "redundancy circuit;" pages 41 and 50 have been amended to refer to "M" before reference numbers 1825 and 2120; Fig. 19 has been amended to delete reference to del,1:6>, Ineg<0:2>, RO_div64, Ipos<0:2>, and FEEDBACK; no change has been made in Fig. 19 with respect to StartH, because the term is used on page 46, line 20; no change has been made in Fig. 21 with respect to reference number 2150, because the number is referred to on page 50, line 7; and Fig. 22B has been amended to delete terms MN11 and MN21. In summary, the drawings are believed to be in compliance

with 37 CFR 1.84(p)(5). Copies of the referenced drawing Figs. with proposed amendments have been provided with this Amendment A.

Responding to paragraph 3 of the Office Action, the drawings show every feature of the subject matter of the pending claims as explained in more detail in response to paragraphs 4-5.

Responding to paragraphs 4-5 of the Office Action, the rejection of claims 1-17 under 35 USC § 112 as being indefinite for failing to read on the drawings is respectfully traversed. Claims 1, 2 and 4 read on the embodiment shown in Fig. 8 and described on pages 32-33 as follows (claims 3 and 5 have been cancelled):

Limitations of Claims 1, 2 and 4	Corresponding Parts of Fig. 8
1. An address decoder for a memory cell, comprising:	Fig. 8 shows a decoder as stated in the legend of Fig. 8 and on page 8, lines 10-11. An output of the decoder is word line 804 (Fig. 8, page 32, line 26. As shown in Fig. 1, the outputs of the word line decoders are coupled to memory cells 103 (page 8, lines 22-30).
a. a synchronous portion, disposed to receive and respond to a clocked signal;	The synchronous portion reads on input 802 that is synchronized to a clock (page 32, lines 13-14).
b. an asynchronous portion, coupled with a line for the memory cell; and	The asynchronous portion reads on output 804 that is asynchronous because it is isolated from inputs 802 and 803 that are

	synchronous (page 32, lines 13-14 and 32-34) and because output 804 can be "independently reset" (page 32, line 26).
c. a feedback-resetting portion, coupled with the synchronous portion and the asynchronous portion and interposed there between, the feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion responsive to an asynchronous reset signal.	The feedback-resetting portion reads on the circuitry of Fig. 8 between inputs 802 and 803 and output 804. The isolating of the inputs from the output is described at page 32, lines 32-24. The reset signal reads on the signal at node 810 which is part of a "feedback-resetting loop" (page 32, lines 30-34).
2. The decoder of Claim 1, wherein the feedback-resetting portion substantially isolates the synchronous portion from the asynchronous portion responsive to a monitor signal.	The monitor signal reads on the signal at node 810, which is described as a "monitor node" (page 32, line 33).
4. The decoder of Claim 1, wherein the decoder is an asynchronously-resettable row decoder.	The row decoder is shown in Fig. 1 as row address decoder 110 (page 8, line 30).

Claims 6-10 read on the embodiments shown in Figs. 12, 16 and 17 and described on pages 39-40 as follows:

Limitations of Claims 6-10	Corresponding Parts of Figs. 12, 16 and 17
6. A decoder in a memory module having a plurality of memory cell groups, comprising:	As explained on page 39, lines 32-33 and page 39, line 34-page 40, line 2, Fig. 17 illustrates a preferred embodiment of selector 1600 in Fig. 16 and the module level redundancy decoder of Fig. 12. As explained on page 39, lines 20-24, the selector of Fig. 16 also is suitable for implementing the embodiment shown in Fig. 12. Fig. 12 illustrates memory modules 1201 including a plurality of memory cell groups in redundant memory columns 1206 and 1208. The decoder reads on the global word decoder (GWD) element of Fig. 12., the decoder circuit 1605 of Fig. 16 (page 39, line 25) and the global decoder 1700 of Fig. 17 (page 40, line 2).
a. a signal input;	The signal input reads on the inputs to the GWD element of Fig. 12, the input word line 1650 of Fig. 16 and the inputs of Fig. 17, such as x1 and x2_n.

b. a first memory output coupled with a first memory cell group;	The first memory output reads on the output of the LWD element that is coupled to the memory cell groups in columns 1206 and 1208 (Fig. 12) and the memory cell group of Fig. 1; the output 1670 or first local line 1680 of Fig. 16, which, as shown in Figs. 12 and 1, is coupled to a memory cell group, and output 1706 (Fig. 17), which, as shown in Figs. 12 and 1, is coupled to a memory cell group.
c. a second memory output coupled with a second memory cell group; and	The second memory output reads on the second local word line 1660 of Fig. 16, which, as shown in Figs. 12 and 1, is coupled to a second memory cell group; the second memory output also reads on output 1705 of Fig. 17, which, as shown in Figs. 12 and 1 is coupled to a second memory cell group. In addition, page 40, lines 3-12 state: "In general, decoder 1700 can be coupled with a first, designated memory row, and a second, alternative memory row... Although row decoder 1700 decodes the first memory row under

	normal operations, it also is disposed to select and decode the second memory row in responsive [sic.] to an alternative-row-select signal."
d. a selector coupled between the signal input, the first memory output, and the second memory output, wherein the decoder decodes the first memory cell group, and being disposed to select and decode the second memory cell group responsive to a group-select signal.	The selector reads on the multiplexer 1610 and selector device 1620 of Fig. 16. The group-select signal reads on activation signal 1630 to selector 1600, and the decoder reads on decoder 1605 of Fig. 16. Alternatively, the selector reads on circuit 1700 of Fig. 17. The group-select signal reads on the signals present on inputs 1701 and 1702 (page 40, lines 9-19).
7. The decoder of Claim 6, wherein the selector comprises a multiplexer, the multiplexer selecting to decode from one of the first memory cell group and the second memory cell group, the multiplexer being responsive to the group-select signal.	The multiplexer reads on multiplexer 1610 (Fig. 16), which is responsive to the activation signal 1630.
8. The decoder of Claim 6, wherein the decoder is a row decoder disposed in a memory module having a plurality of	The decoder reads on the Fig. 17 decoder. Page 40, lines 3-12 state: "In general, decoder 1700 can be coupled with a first,

adjacent memory rows, and wherein a first memory row and a second memory row are adjacent memory rows in the memory module, and the group-select signal is an alternative-row-select signal.	designated memory row, and a second, alternative memory row. Although the second row may be a physical row adjacent the first memory row, and another of the originally designated rows of the memory module, the second row also may be a redundant row which is implemented in the module. Although row decoder 1700 decodes the first memory row under normal operations, it also is disposed to select and decode the second memory row in responsive [sic.] to an alternative-row-select signal."
9. The decoder of Claim 6, wherein the decoder is a column decoder disposed in a memory module having a plurality of adjacent memory columns, and wherein a first memory column and a second memory column are adjacent memory columns in the memory module, and the group-select signal is an alternative-column-select signal.	The column decoder reads on the Fig. 16 embodiment. In connection with Fig. 16, the specification teaches at page 39, lines 20-24: "Selector 1600 is suitable for implementing module-level redundancy, such as that described relative to module 1200 in FIG. 12, which may be row redundancy or column redundancy for a given implementation." The adjacent memory columns are shown in Fig. 12.

10. The decoder of Claim 6, wherein the decoder is a row decoder disposed in a memory module having assigned memory rows and a redundant memory row, and wherein the first memory row is an assigned memory row, the second memory row is the redundant memory row and the group-select signal is a redundant-row-select signal.	This claim reads on the Fig. 17 embodiment which is explained on page 40, lines 3-15 as follows: "In general, decoder 1700 can be coupled with a first, designated memory row, and a second, alternative memory row. Although the second row may be a physical row adjacent the first memory row, and another of the originally designated rows of the memory module, the second row also may be a redundant row which is implemented in the module. Although row decoder 1700 decodes the first memory row under normal operations, it also is disposed to select and decode the second memory row in responsive [sic.] to an alternative-row-select signal. Where the second row is a redundant row, it may be more suitable to deem the selection signal to be a 'redundant-row-select' signal. The aforementioned row select signals are illustrated as inputs 1701 and 1702."

Claims 12-16 have limitations in common with earlier claims and read on embodiments as described in connection with the earlier claims as follows:

12. A decoder in a memory module having a plurality of memory cell groups, comprising:	This preamble is identical to the preamble of claim 6 and reads on the same subject matter as the preamble to claim 6.
a. a synchronous portion, disposed to receive and respond to a clocked signal;	This limitation is identical to limitation a of claim 1, and reads on the same subject matter as limitation a of claim 1.
b. an asynchronous portion, coupled with a selected memory cell group;	This limitation is substantially identical to limitation b of claim 1, and reads on the same subject matter as limitation b of claim 1.
c. a feedback-resetting portion, coupled with the synchronous portion and the asynchronous portion and interposed there between, the feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion responsive to an asynchronous reset signal;	This limitation is identical to limitation c of claim 1, and reads on the same subject matter as limitation c of claim 1.
d. a signal input;	This limitation is identical to limitation a of claim 6, and reads on the same subject

	matter as limitation a of claim 6.
e. a first memory output coupled with a first memory cell group;	This limitation is identical to limitation b of claim 6, and reads on the same subject matter as limitation b of claim 6.
f. a second memory output coupled with a second memory cell group; and	This limitation is identical to limitation c of claim 6, and reads on the same subject matter as limitation c of claim 6.
g. a selector coupled between the signal input, the first memory output, and the second memory output, wherein the decoder decodes the first memory cell group, and being disposed to select and decode the second memory cell group responsive to a group-select signal.	This limitation is identical to limitation d of claim 6, and reads on the same subject matter as limitation d of claim 6.
13. The decoder of Claim 12, wherein the selector comprises a multiplexer, the multiplexer selecting to decode from one of the first memory cell group and the second memory cell group, the multiplexer being responsive to the group-select signal.	This claim is substantially identical to claim 7 and reads on the same subject matter as claim 7.
14. The decoder of Claim 12, wherein the decoder is a row decoder disposed in a	This claim is substantially identical to claim 8 and reads on the same subject matter as

memory module having a plurality of adjacent memory rows, and wherein a first memory row and a second memory row are adjacent memory rows in the memory module, and the group-select signal is an alternative-row-select signal.	claim 8.
15. The decoder of Claim 12, wherein the decoder is a column decoder disposed in a memory module having a plurality of adjacent memory columns, and wherein a first memory column and a second memory column are adjacent memory columns in the memory module, and the group-select signal is an alternative-column-select signal.	This claim is substantially identical to claim 9 and reads on the same subject matter as claim 9.
16. The decoder of Claim 12, wherein the decoder is a row decoder disposed in a memory module having assigned memory rows and a redundant memory row, and wherein the first memory row is an assigned memory row, the second memory row is the redundant memory row and the group-select signal is a redundant-	This claim is substantially identical to claim 10 and reads on the same subject matter as claim 10.

row-select signal.	

Responding to paragraphs 6-7 of the Office Action, the rejection of claims 1-17 under 35 U.S.C. § 102(e) as being anticipated by Ooishi (U.S. Patent No. 6,363,030) is respectfully traversed. The Examiner relies on Fig. 19 of Ooishi, which is described as a diagram showing a configuration of the Fig. 16 frequency dividing circuit 4040 (Col. 3, lines 42-43). Fig. 16 is described as a diagram of an internal clock (Col. 3, lines 34-36). Thus, the components shown in Fig. 19 are part of a clock, not an address decoder for a memory cell as claimed. Since limitation b of claim 1 refers to the "memory cell" portion of the preamble, the preamble is properly construed as a limitation of the claim against which the prior art is measured.

Limitation a of claim 1 recites a synchronous portion of the claimed address decoder for a memory cell. The synchronous portion is disposed to receive and respond to a clocked signal. Aside from the fact that Fig. 19 of Ooishi is used to generate a clock signal, there appears to be no relationship between the address decoder of claim 1 and Fig. 19 of the Ooishi Patent. Fig. 19 does not teach a synchronous portion of an address decoder, an asynchronous portion of an address decoder, or a feedback-resetting portion of an address decoder as claimed. For all these reasons, Ooishi does not anticipate claim 1 under 35 U.S.C. § 102(e).

Regarding claim 6, Ooishi does not appear to teach a selector of the type claimed. As far as the undersigned can determine, the Examiner does not purport to find any such teaching in Ooishi. As a result, claim 6 also is not anticipated under 35 U.S.C. § 102(e).

Claim 12 includes limitations found in claims 1 and 6. As a result, claim 12 also is not anticipated under 35 U.S.C. § 102(e).

Claims 2 and 4 are dependent on claim 1 and are allowable for the foregoing reasons.

Claims 7-10 are dependent on claim 6 and are allowable for the foregoing reasons.

Claims 13-16 are dependent on claim 12 and are allowable for the foregoing reasons.

In summary, each of claims 1-2, 4, 6-10 and 12-16 is allowable, and such action is respectfully requested.

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Respectfully submitted,

Ronald E. Larson
Reg. No. 24,478
Attorney for Applicant

McAndrews, Held & Malloy, Ltd.
500 W. Madison, 34th Floor
Chicago, IL 60661
312.775.8000